

**REMARKS**

Claims 1 to 23 were pending in the application at the time of examination.

The Examiner subjected Claims 1 to 20 and 21 to 23 to a restriction requirement and Applicants elected Claims 1 to 20. The Examiner rejected Claims 1 to 20 under the judicially created doctrine of obviousness-type double patenting over Claims 1 to 24 of U.S. Patent Application US 2003/0154365 A1. The Examiner rejected Claims 1 to 5 and 16 to 20 under 35 U.S.C. 102(b) as anticipated by the Kanazashi et al. reference.

The Examiner rejected Claims 2 to 5 and 17 to 20 under 35 U.S.C. 103(a) as obvious over the Kanazashi et al. reference in view of the Wallace Steven et al. reference.

Applicants hereby elect the Examiner's "Invention I", Claims 1 to 20. Applicants include herewith a "Terminal Disclaimer to Obviate a Double Patenting Rejection Over a Prior Patent Including Statement Under 37 CFR 3.73(b)". Applicants have cancelled Claims 2 and 17, without prejudice. Applicants have amended Claims 1, 3, 16 and 18. Consequently, Claims 1, 3 to 16, and 18 to 20 remain in the Application.

**ELECTION OF CLAIMS 1 TO 20**

The Examiner subjected Claims 1 to 20 and 21 to 23 to a restriction requirement and Applicants verbally elected Claims 1 to 20.

Applicants hereby officially elect the Examiner's "Invention I", Claims 1 to 20, and withdraw Claims 21, 22 and 23.

**REJECTION OF CLAIMS 1 TO 20 UNDER THE JUDICALLY CREATED  
DOCTRINE OF OBVIOUSNESS-TYPE DOUBLE PATENTING**

The Examiner rejected Claims 1 to 20 under the judicially created doctrine of obviousness-type double patenting over Claims 1 to 24 of U.S. Patent Application US 2003/0154365 A1.

Applicants include herewith a "Terminal Disclaimer to Obviate a Double Patenting Rejection Over a Prior Patent Including Statement Under 37 CFR 3.73(b)". In light of the submitted "Terminal Disclaimer to Obviate a Double Patenting Rejection Over a Prior Patent Including Statement Under 37 CFR 3.73(b)", Applicants respectfully request the Examiner withdraw the rejection of Claims 1 to 20 under the judicially created doctrine of obviousness-type double patenting over Claims 1 to 24 of U.S. Patent Application US 2003/0154365 A1.

In addition, Applicants note that the only rejection cited against Claims 6 to 15 was the rejection based on double-patenting over Claims 1 to 24 of U.S. Patent Application US 2003/0154365 A1. Consequently, in light of the submitted "Terminal Disclaimer to Obviate a Double Patenting Rejection Over a Prior Patent Including Statement Under 37 CFR 3.73(b)", Applicants respectfully request the Examiner allow Claims 6 to 15 to issue.

REJECTION OF CLAIMS 1 TO 5 AND 16 TO 20 UNDER 35 U.S.C.

102(a)

The Examiner rejected Claims 1 to 5 and 16 to 20 under 35 U.S.C. 102(b) as anticipated by the Kanazashi et al. reference.

Claims 2 and 17 have been cancelled, without prejudice. Consequently, Applicants respectfully submit the rejection of Claims 2 and 17 is now moot except to the extent elements of Claims 2 and 17 have been incorporated into Claims 1 and 16, as amended, and as discussed below.

Applicants have amended Claims 1 and 16. Applicants' Claim 1, as amended, recites, with emphasis added:

A modified glitch latch, said modified glitch latch being a sensing element coupled to a read word line of a retirement payload array, said modified glitch latch comprising:

a modified glitch latch output terminal;

a control circuit, said control circuit comprising a control circuit first input terminal, a control circuit second input terminal and a control circuit output terminal;

a clock signal coupled to said control circuit first input terminal, said clock signal having a first or "A" phase and a second or "B" phase;

a read signal coupled to said control circuit second input terminal, said read signal having a first or inactive phase and a second or active phase, said second or active phase of said read signal corresponding to a shift in position of a read pointer of said retirement payload array, wherein;

a control signal from said control circuit output terminal opens said modified glitch latch only when, both:

said clock signal is in said "B" phase; and  
said read signal is in said active phase.

Applicants' Claim 16, as amended, recites, with emphasis added:

A method for controlling the operation of a modified glitch latch, said glitch latch being a sensing element coupled to a read word line of a retirement payload array, said method comprising:

receiving a clock signal, said clock signal having a first or "A" phase and a second or "B" phase;

receiving a read signal, said read signal having a first or inactive phase and a second or active phase, said second or active phase of said read signal corresponding to a shift in position of a read pointer of said retirement payload array; and

opening said modified glitch latch only when, both:

said clock signal is in said "B" phase;

and said read signal is in said active phase.

As seen above, both of Applicants' independent Claims 1 and 16, as amended, includes the recited limitations "said glitch latch being a sensing element coupled to a read word line of a retirement payload array" and "said second or active phase of said read signal corresponding to a shift in position of a read pointer of said retirement payload array".

Applicants respectfully submit that the Kanazashi et al. reference fails to disclose, teach or suggest "said glitch latch being a sensing element coupled to a read word line of a retirement payload array" or "said second or active phase of said read signal corresponding to a shift in position of a read pointer of said retirement payload array" as recited in Applicants' Claims 1 and 16, as amended. Consequently, Applicants respectfully submit that Claims 1 and 16, as amended, are patentable over the Kanazashi et al. reference and Applicants respectfully request the Examiner withdraw the rejection of Claims 1 and 16 as anticipated by the Kanazashi et al. reference and allow Claims 1 and 16 to issue.

The Examiner also rejected Claims 2, 3, 4, and 5 and Claims 17, 18, 19 and 20 as anticipated by the Kanazashi et al. reference. However, at paragraph 5, on page 8, of the Official

Action mailed February 24, 2005, the Examiner then states that Kanazashi et al. "does not teach explicitly use with a read word line of a retirement payload array." Given this statement, and the correctness of this statement, it is not clear to Applicants' Attorney how the Examiner came to the conclusion that rejection of Claims 2, 3, 4, 5, 17, 18, 19 and 20 under 35 U.S.C. 102 was justified.

However, Claims 3, 4, 5 and 18, 19 and 20, depend, directly or indirectly, on Claims 1 and 16, as amended, respectfully, and therefore include all of the features and limitations of their respective parent Claims 1 and 16, as amended. Consequently, Applicants respectfully submit that Claims 3, 4, 5, 18, 19, and 20 are also patentable over the Kanazashi et al. reference for at least the reasons discussed above and Applicants respectfully request the Examiner withdraw the rejection of Claims 3, 4, 5 and 18, 19 and 20 as anticipated by the Kanazashi et al. reference.

**REJECTION OF CLAIMS 2 TO 5 AND 17 TO 20 UNDER 35 U.S.C**  
**103(b)**

The Examiner rejected Claims 2 to 5 and 17 to 20 under 35 U.S.C. 103(a) as obvious over the Kanazashi et al. reference in view of the Wallace Steven et al. reference.

Claims 2 and 17 have been cancelled, without prejudice. Consequently, Applicants respectfully submit the rejection of Claims 2 and 17 is now moot except to the extent elements of Claims 2 and 17 have been incorporated into Claims 1 and 16, as amended, and as discussed below.

Applicants have amended Claims 1 and 16 to incorporate elements of Claim 2 into Claim 1 and elements of Claim 17 into Claim 16. Applicants' Claim 1, as amended, recites, with emphasis added:

A modified glitch latch, said modified glitch latch being a sensing element coupled to a read word line of a retirement payload array, said modified glitch latch comprising:

a modified glitch latch output terminal;

a control circuit, said control circuit comprising a control circuit first input terminal, a control circuit second input terminal and a control circuit output terminal;

a clock signal coupled to said control circuit first input terminal, said clock signal having a first or "A" phase and a second or "B" phase;

a read signal coupled to said control circuit second input terminal, said read signal having a first or inactive phase and a second or active phase, said second or active phase of said read signal corresponding to a shift in position of a read pointer of said retirement payload array, wherein;

a control signal from said control circuit output terminal opens said modified glitch latch only when, both:

said clock signal is in said "B" phase; and

said read signal is in said active phase.

Applicants' Claim 16, as amended, recites, with emphasis added:

A method for controlling the operation of a modified glitch latch, said glitch latch being a sensing element coupled to a read word line of a retirement payload array, said method comprising:

receiving a clock signal, said clock signal having a first or "A" phase and a second or "B" phase;



receiving a read signal, said read signal having a first or inactive phase and a second or active phase, said second or active phase of said read signal corresponding to a shift in position of a read pointer of said retirement payload array; and  
opening said modified glitch latch only when, both:  
said clock signal is in said "B" phase;  
and said read signal is in said active phase.

As seen above, both of Applicants independent Claims 1 and 16, as amended, includes the recited limitations "**said second or active phase of said read signal corresponding to a shift in position of a read pointer of said retirement payload array**".

The Examiner has invoked the Wallace Steven reference as an example of a retirement payload array. However, Applicants respectfully submit that the Examiner has failed to show where in the Kanazashi et al. reference, the Wallace Steven reference, or any combination of the Kanazashi et al. reference and the Wallace Steven reference, it is disclosed, taught or suggested "**said second or active phase of said read signal corresponding to a shift in position of a read pointer of said retirement payload array**", as recited in Applicants Claims 1 and 16, as amended. Consequently, Applicants respectfully submit that Claims 1 and 16, as amended, are patentable over the Kanazashi et al. reference, the Wallace Steven reference, or any proper combination of the Kanazashi et al. reference and the Wallace Steven reference, for at least this reason. Consequently, Applicants respectfully request the Examiner allow Claims 1 and 16, as amended, to issue.

Claims 3, 4, 5 and 18, 19 and 20, depend, directly or indirectly on Claims 1 and 16, as amended, respectfully, and therefore include all of the features and limitations of their respective parent Claims 1 and 16, as amended. Consequently,

Appl. No. 10/083,931

Amdt. dated July 25, 2005

Reply to Office Action of February 24, 2005

Applicants respectfully submit that Claims 3, 4, 5, 18, 19, and 20 are also patentable over the Kanazashi et al. reference, the Wallace Steven reference, or any proper combination of the Kanazashi et al. reference and the Wallace Steven reference, for at least the reasons discussed above and Applicants respectfully request the Examiner withdraw the rejection of Claims 3, 4, 5 and 18, 19 and 20 under 35 U.S.C. 103(a) as obvious over the Kanazashi et al. reference. (US 6,337,833 B1) in view of the Wallace Steven et al. reference and allow Claims 3, 4, 5 and 18, 19 and 20 to issue.

#### CONCLUSION

For the foregoing reasons, Applicants respectfully request allowance of all pending claims. If the Examiner has any questions relating to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicants.

#### **CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on July 25, 2005.



Attorney for Applicants

July 25, 2005

Date of Signature

Respectfully submitted,



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